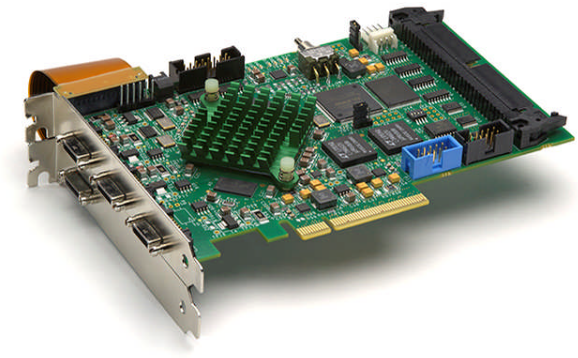
Axion-CL

BitFlow's 6th Generation Camera Link Frame Grabbers

BitFlow has been making Camera Link frame grabbers since 1999. With each successive generation of frame grabbers, BitFlow has improve the quality, flexibility and robustness of their interfaces. Meanwhile, much has changed on the backend; PCI to PCIe, Gen 1 to Gen 2, etc. Also the Camera Link Specification had been continuously evolving: 80-bit (10-tap) mode was added, Power of Camera Link (PoCL), new connectors, new tap formats. Even though the specification has been around a long time, it is still one of the simplest, effecient and least expensive ways to get camera data into a computer. It also benefits from 100s of thousands of pieces of CL equipment sold worldwide.



BitFlow has been on top of all these changes and has continuously improved and updated their Camera Link frame grabbers. The Axion-CL is the culmination of all of this improvements, the most powerful CL frame grabber BitFlow has ever manufactured.

The Axion-CL also benefits from other products in BitFlow's line up. The Axion-CL uses the Cyton-CXP's backend: the StreamSync DMA engine and buffer manager. A brand new PCIe Gen 2 interface, with DMA optimized for modern (fully loaded, fully busy) computers.

The Virtual Frame Grabber

The Axion supports up to two cameras. In dual camera mode, the board looks to Windows and application software like two completely independent frame grabbers. This simplifies the setup for multiple camera as each camera is really treated separately. Of course, the cameras can be internally synchronized if needed, but the can also run completely indepenedently. The two cameras do not have to be the same resolution, frame rate, trigger mode or even tap format.

StreamSync

The StreamSync system consists of an Acquisition Engine and a Buffer Manager. The StreamSync system was first released on the Cyton-CXP and is a departure from previous BitFlow frame grabbers. The StreamSync system is a start-from-scratch complete redesign of the acquisition and DMA parts of a frame grabber. BitFlow used it years of experience in this area to design a next generation, super efficient capture system.

StreamSync Features

- Efficient support for variable sized images with fast context switches between frames
- Per frame control of acquisition properties (AOI specifically)
- Hardware control of image sequencing
- Enhanced debug capabilities
- Efficient support for on-demand buffer allocation (Genicam model)

Gracefully recovery from dropped packets (either on the input side or the DMA side)

PCI Express Gen 2.0 Interface

The Cyton-CXP has a Gen 2.0 x8 PCI Express bus interface. The Gen 2.0 PCIe bus doubles the data rate of the Gen 1.0 bus while using the same footprint and connectors. The Cyton-CXP is fully backwards compatible with Gen 1.0 motherboards, though the data rate will be halved. However, Gen 2.0 motherboards have been shipping for a few years and will be the norm on almost all motherboards looking forward. The board will work in any slot that it fits in. This means not only x16 and x8 slots, but also, as is becoming the trend, x4 and x1 slots that use x16 connectors. Performance will be degraded in x1 and x4 slots, but the board will work fine in applications that don't require maximum data rate.

Camera Control and I/O

I/O signals can be routed to/from many internal and external destinations, the flexibility of the routing is unprecedented in the industry. In addition, there are separate hardware I/O signals which can be connected to/from external source. Finally each CL camera has a full set of these signals which can be run independently. The Axion-CL board, as with our past interface products, supports not only simple triggering modes but also complicated, application-specific triggering and control interactions with your hardware environment.

Powerful Camera Configuration Files

Unlike previous BitFlow products, the Gen 2 products use an XML base camera configuration file. These files can be edited in any text editor. The file format is fully documented (see the downloads page). The XML file format is unique in that very few items are needed in order to get the board up and running with a given camera, which still supporting a rich set of tokens for very customized support of the board and/or camera. The XML camera files also support multiple modes for a given camera. This simplifies file management as only one file is needed for a particular make/model of a camera. All of its modes are supported internally by the token in the XML file.

Application Support

Adding the Axion-CL to your application is simple with our SDK, which supports both 32-bit and 64-bit operating systems. Applications can be developed using C/C++/.NET and our sophisticated buffer management APIs. In addition, free drivers can be download from our web site for most 3rd party machine vision packages. The Cyton models are software compatible with each other, as well as with all the other current BitFlow frame grabbers. This makes migrating applications from Camera Link or analog to CXP simple and quick.

- Half-Size x4 PCI Gen 2.0 Express Board
- Camera Link 2.0 Compliant
- Supports up to two cameras
- Supports base, medium, full, 80-bit (10-tap) CL cameras
- Supports CL clocks up to 85 MHz
- Supports simultaneous capture two 80-bit/85 MHz cameras
- Industry standard SDR Camera Link connectors
- Support PoCL and non-PoCL cameras
- Support dual connector PoCL
- Provides Safe Power, full protection from all power line faults
- Cameras can be accurately synchronized, or can be completely independent
- PCI Express x4 Gen 2.0 interface (also works in x8 and x16 slots)
- Compatible with PCI Epress Gen 1.0 slots
- Separate I/O for each camera
- Highly deterministic, low latency frame grabber to camera trigger
- Supports simultaneous communications to all cameras
- Windows "sees" a separate frame grabber for each camera
- FlowThru technology means no on-board memory is needed
- StreamSync acquisition engine optimizes synchronization between acquisition and DMA
- StreamSync buffer manager maximize DMA channel efficiency
- Acquire variable length frames from line scan cameras
- Acquire image sequences well beyond the 4GB barrier
- No frame rate limit
- Triggers and encoders for external control of acquisition
- Programmable signal generator for camera control (independent for each camera)
- Quadrature encoder support including sophisticated triggering schemes
- Encoder divider/multiplier
- Drivers, utilities and examples for Windows and Linux
- Supported on both 32-bit and 64-bit platforms
- Drivers for most 3rd party processing environments (e.g. HALCON, LabView, VisionPro, MA-TLAB, etc.)
- Full GenICam support for control and capture
- RoHS compliant

AXN-PC2-CL-2xE

- Two base/medium/full/80-bit cameras
- PoCL on both connectors for both cameras

AXN-PC2-CL-1xE

- One base/medium/full/80-bit cameras
- PoCL on both connectors

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